Amendments to the Claims

Kindly amend claims 1-5 & 7-9 as set forth below. All pending claims are reproduced below, with changes in the amended claims shown by underlining (for added matter) and strikethrough/double brackets (for deleted matter).

1. (Currently Amended) A method for forming an output reception ~~pulses~~ pulse in a receiver operating according to the Fast InfraRed (FIR) IrDA standard wherein an input signal from ~~output signals of~~ an upstream comparator that recognizes light pulses is ~~are~~ newly formed and output as the output reception pulse ~~pulses~~ for evaluation by means of a downstream arrangement, wherein: in a first step, ~~an~~ the input signal is delivered by the ~~an~~ upstream comparator; the input signal is delayed by a delay arrangement; generation of a time reference by a time reference generation arrangement controlled by the input signal is started; controlled by the input signal delayed in the first step, forming of an output reception pulse by an output pulse production arrangement is started; upon completion of the generation of the time reference, an examination of a level of the input signal is conducted which carries out a back-reference to duration of the output reception pulse; and subject to results of the examination, the duration of the output reception pulse is adjusted by the output pulse production arrangement, wherein duration of the output reception pulse is independent of actual pulse duration of the input signal delivered by the upstream comparator.

2. (Currently Amended) The method according to claim 1, wherein the delay by the delay arrangement of the input signal delivered by the upstream comparator is done in a first and a second partial step and that between the first and second partial steps, a regeneration of the signal is carried out.

3. (Currently Amended) The method according to claim 1, wherein the generation of the time reference by the time reference generation arrangement is started by the input signal or the input signal delayed in a first partial step.

4. (Currently Amended) The method according to claim 1, wherein the forming of the output pulse by the output pulse production arrangement is done such that forming of a first pulse and a second pulse is started in parallel and subject to the examination of the input signal level either the first or the second pulse is emitted at the output.

5. (Currently Amended) An arrangement for forming an output reception ~~signals~~ pulse in a receiver operating according to the Fast InfraRed (FIR) IrDA standard wherein ~~the output signals of~~ an input comparator signal from an upstream comparator that recognizes light pulses is ~~are~~ newly formed for evaluation by a downstream arrangement, wherein an input of a delay arrangement is connected to an output of the upstream comparator ~~an input of the arrangement for forming reception pulses INP~~, for supply of [[a]] the input comparator signal, wherein a first output of the delay arrangement is connected to a first input of a down stream output pulse producing arrangement and a second output of the delay arrangement is connected to a time reference generating arrangement, the first output and the second output being different outputs of the delay arrangement, wherein an output of the time reference generating arrangement is connected to a second input of the output pulse producing arrangement and, wherein an output of the output pulse producing arrangement is connected to the output OUT of the arrangement for forming the output reception pulse, wherein duration of the output reception pulse is adjusted by the output pulse producing arrangement, and duration of the output reception pulse is independent of actual pulse duration of the input comparator signal. ~~pulses.~~

6. (Previously Presented) The arrangement according to claim 5, wherein the delay arrangement is comprised of a series connection of a first and a second delay arrangement parts and an arrangement for pulse reconstruction installed between the first and second delay arrangements parts.

7. (Currently Amended) The arrangement according to Claim 5, wherein the output pulse producing arrangement is comprised of a circuit for forming a first pulse, a circuit for forming a second pulse, ~~impulse,~~ a circuit for examining the input signal level and a selection circuit .

8. (Currently Amended) The arrangement according to claim 6 wherein the delay arrangement comprises a p-channel transistor whose gate contact is connected to an input of a logical NAND circuit and via a negator to ~~an~~ a primary input ~~"Input"~~ whose source contact is connected to a potential VDD ~~VDDa~~ and whose drain contact is connected to an input IBIA of the delay arrangement and to the input of a Schmitt trigger, a Schmitt trigger whose negated output is connected to a second input ~~output~~ of the logical NAND circuit and the logical NAND circuit whose negative output is connected to ~~an~~ a primary output of the delay arrangement ~~"Output"~~.

9. (Currently Amended) The arrangement according to claim 6, wherein in an arrangement for pulse construction and for forming a first pulse, a second pulse and the time reference generation, a respective primary input ~~"Input"~~ is connected to a negator, wherein an output of the negator is connected to a first input of a downstream first NAND circuit and a series connection comprised of three negators whose output is connected to a second input of the first NAND circuit, wherein an output of the first NAND circuit is connected to a first input of a second NAND circuit, wherein an input IBIA of the arrangement is connected to a drain contact of a p-channel transistor and is connected via a Schmitt-trigger to a first input of a NOR circuit, wherein an input POC of the arrangement is connected to a second input of the NOR circuit, wherein an output of the NOR circuit is connected to a first input of a third NAND circuit, wherein an output of the third NAND circuit is connected to the second input of the second NAND circuit, via a negator to a gate contact of the p-channel transistor whose source contact is connected to a potential VDDa, and to ~~an~~ a primary output ~~"Output"~~ of the arrangement and wherein an output of the second NAND-circuit is connected to a second input of the third NAND circuit.

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